WHAT IS CLAIMED IS:

1. A decoder structure with m*n nodes, each of said nodes comprising a plurality of transistor nodes and a plurality of channel nodes, one of said transistor nodes N(i1, j1) corresponding to a transistor area A(i1,j1), and one said channel nodes N(i2,j2) corresponding to a channel area A(i2,j2), wherein $1 \leqq i1, i2 \leqq m$, $1 \leqq j1, j2 \leqq n$, $i1 \neq i2$, $j1 \neq j2$, said decoder structure comprising:

a substrate;

a first source/drain region and a second source/drain region formed within said substrate in said transistor area A(i1, j1);

a channel formed within said substrate in said channel area A(i2, j2);

a first insulating layer formed on said first source/drain region, said second source/drain region and said channel;

a gate formed on said first insulating layer between said first source/drain region and said second source/drain region;

a second insulating layer formed on said gate; and

a metal layer formed over said gate and electrically connected with said gate;

wherein

when said transistor node N(i1, j1) is next to said channel node N(i2, j2) on the same row, one of said first source/drain region and said second source/drain region of said transistor area A(i1, j1) is connected with said channel of said channel area A(i2, j2);

when said transistor node N(i1, j1) is next to said transistor node N(i3, j3) on the same row, one of said first source/drain region and said second source/drain region of said transistor node N(i1, j1) is connected with said one of first source/drain

region and said second source/drain region of said transistor node N(i3, j3);

when said channel node N(i2, j2) is next to said channel node N(i4, j4) on the same row, said channel of said channel node N(i2, j2) is connected with said channel of said channel node N(i4, j4); and

said metal layer electrically connecting said gates of said transistor nodes on the same column to form a plurality of decoder input for receiving digital signal data.

2. The decoder structure of claim 1, wherein said first insulating layer is an oxide layer.

3. A method for manufacturing a decoder with m*n nodes, said m*n nodes comprising p transistor nodes and (m*n-p) channel nodes, said transistor nodes corresponding to a transistor area, said channel nodes corresponding to a channel area, p is an integer smaller than m*n, said method comprising:

providing a substrate;

forming an insulating layer on said substrate;

forming p gates on said transistor area;

forming p first sources/drains and p second sources/drains on said transistor area, and forming (m*n-p) channels on said channel area to form m signal lines;

forming a second insulating layer; and

forming n decoder inputs on said second insulating layer, said decoder inputs electrically connected with said gates by a plurality of contacts.

4. The method of claim 3, wherein said first insulating layer is an oxide layer.

5. A decoder structure with a plurality of transistor nodes and a plurality of channel nodes, one of said transistor nodes corresponding to a transistor area and one

of said channel nodes corresponding to a channel area, said decoder structure comprising:

a substrate;

a transistor disposed in said transistor area, said transistor comprising a gate, source/drain regions, said source/drain regions formed within said substrate beside said gate;

a metal layer disposed on said gate and insulated with said substrate;

a channel formed within said substrate in said channel area;

when a first transistor node of said transistor nodes is connected to a first channel node of said channel nodes on the same row, one of said source/drain regions of said transistor area is connected with said channel of said channel area;

when said first transistor node of said transistor nodes is connected to a second transistor node of said transistor nodes on the same row, one of source/drain regions of said first transistor node is connected with one of source/drain regions of said second transistor node;

when said first channel node is connected to a second channel node of said channel nodes on the same row, said channel of said first channel node is connected with said channel of said second channel node; and

said metal layer electrically connecting said gates of said transistor nodes on the same column by at least one contact to form a plurality of decoder input for receiving digital signal data.

6. The decoder structure of claim 5 further comprising a first insulating layer between said gate and said substrate to electrically insulate said gate and said substrate.

7. The decoder structure of claim 5 further comprising a second insulating layer between said metal layer and said substrate to insulate said metal layer and said

substrate.

8. The decoder structure of claim 5, wherein said channel area on said substrate does not comprises said gate of said transistor.

9. The decoder structure of claim 5, wherein said metal layer in said channel area is electrically insulated with said channel area.